

# FAN8040

## 4-Channel Motor Driver

### Features

- 4-channel Balanced Transformerless (BTL) Driver
- 3-channels PWM input direct-coupled type include internal filters.
- Separated power supply voltages (PVCC1: CH1 and CH2, PVCC2: CH3 and CH4)
- Built-in input pin selection function of channel 4
- Built-in OP-amplifier
- Built-in Power Save function
- Built-in Thermal Shutdown Circuit (TSD)
- Operating ranges: 4.5~ 13.2V

### Description

The FAN8040G3 is a monolithic integrated circuit, suitable for 4-channel motor driver which drives tracking actuator, focus actuator, sled motor and spindle motor of compact disk player system.



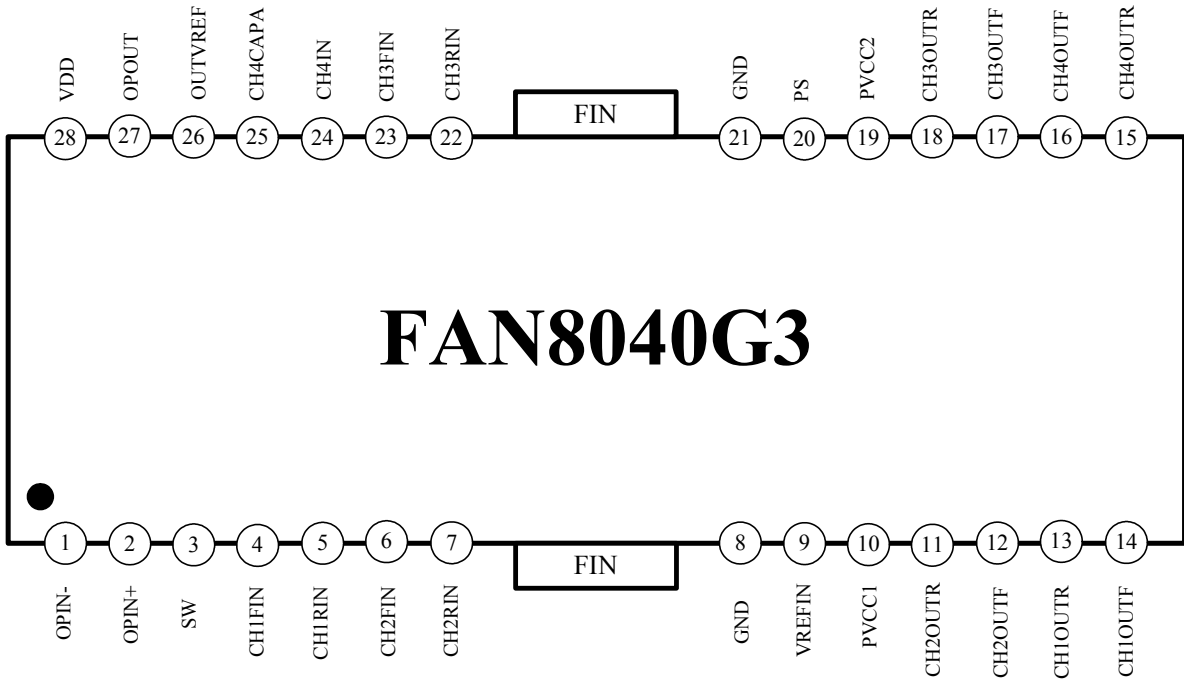
### Typical Applications

- Compact Disk Player (CDP)
- Video Compact Disk Player (VCD)
- Other Compact Disk Media

### Ordering Information

Device	Package	Operating Temp.
FAN8040G3	28-SSOPH-375SG2	-40°C ~ +85°C
FAN8040G3X	28-SSOPH-375SG2	-40°C ~ +85°C

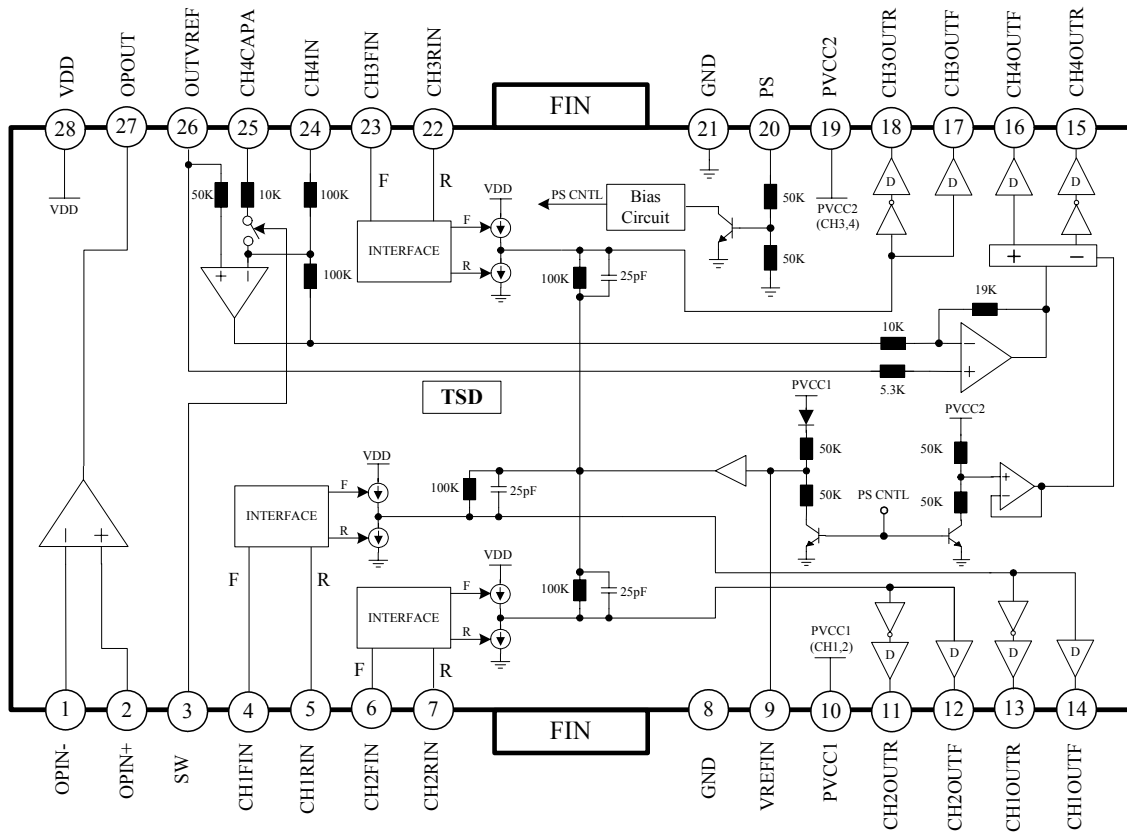
## Pin Assignments



## Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	OPIN-	I	OP-amplifier negative input
2	OPIN+	I	OP-amplifier positive input
3	SW	I	channel 4 input change switch input
4	CH1FIN	I	Channel 1 PWM forward input
5	CH1RIN	I	Channel 1 PWM reverse input
6	CH2FIN	I	Channel 2 PWM forward input
7	CH2RIN	I	Channel 2 PWM reverse input
8	GND	-	Ground 1
9	VREFIN	I	Internal reference voltage input terminal
10	PVCC1	-	Power supply voltage for channel 1 and channel 2
11	CH2OUTR	O	Channel 2 reverse output
12	CH2OUTF	O	Channel 2 forward output
13	CH1OUTR	O	Channel 1 reverse output
14	CH1OUTF	O	Channel 1 forward output
15	CH4OUTR	O	Channel 4 reverse output
16	CH4OUTF	O	Channel 4 forward output
17	CH3OUTF	O	Channel 3 forward output
18	CH3OUTR	O	Channel 3 reverse output
19	PVCC2	-	Power supply voltage for channel 3 and channel 4
20	PS	I	Power save signal input
21	GND	-	Ground 2
22	CH3RIN	I	Channel 3 PWM reverse input
23	CH3FIN	I	Channel3 PWM forward input
24	CH4IN	I	Channel 4 input
25	CH4CAPA	I	Channel 4 external capacitor connection terminal
26	OUTVREF	I	Channel 4 external reference voltage input terminal
27	OPOUT	O	Op-amplifier output
28	VDD	-	Predriver power supply voltage

# Internal Block Diagram

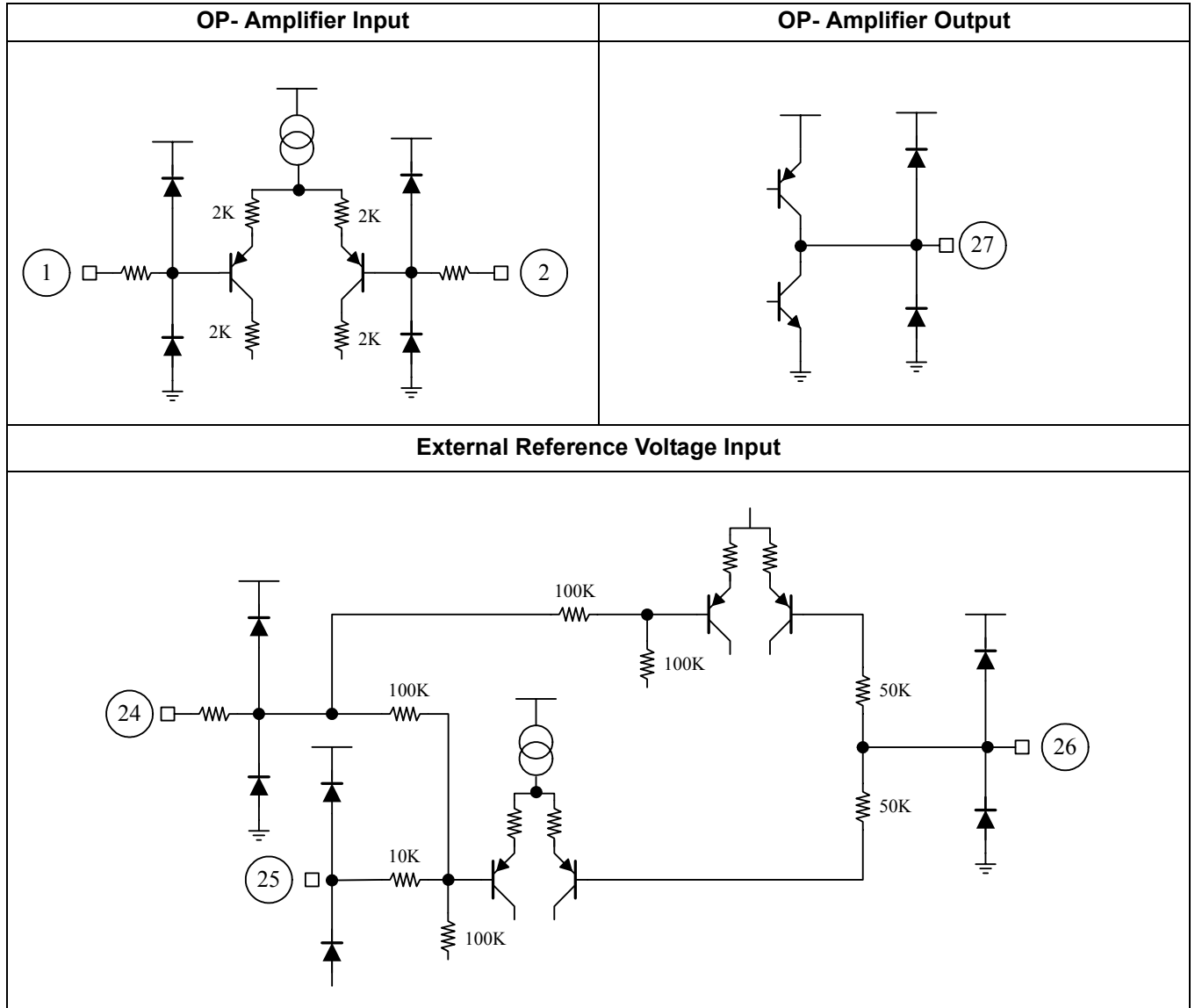


D : Drive Buffer  
 SW : H--> ON, L --> OFF

# Equivalent Circuits

Driver Forward Input	Driver Reverse Input
<p>CH1, CH2 and CH3</p> <p>17K</p> <p>4 6 23</p>	<p>CH1, CH2 and CH3</p> <p>17K</p> <p>5 7 22</p>
Driver Output	Internal Reference Voltage
<p>30K</p> <p>30K</p> <p>11 15</p> <p>12 16</p> <p>13 17</p> <p>14 18</p>	<p>9</p> <p>50K</p> <p>50K</p>
PS Input	CH4 SW Input
<p>20</p> <p>50K</p> <p>50K</p>	<p>3</p> <p>2K</p> <p>50K</p>

**Equivalent Circuits** (Continued)



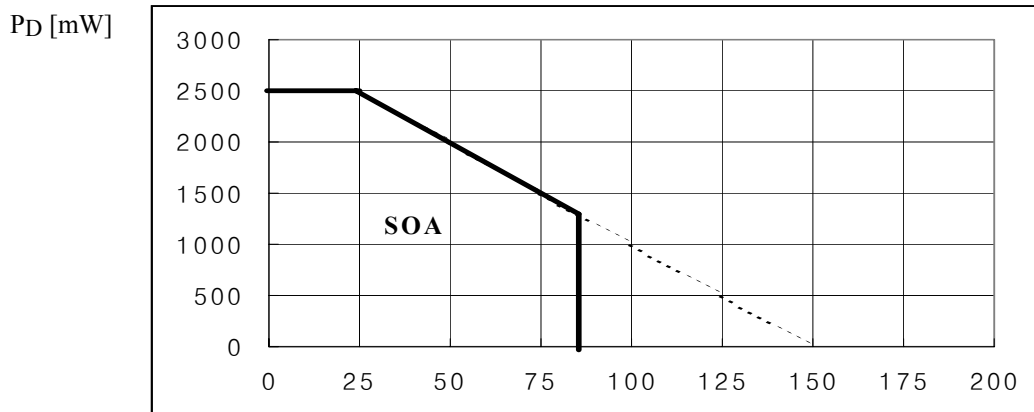
## Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit
Supply Voltage	PVCC1, 2	15	V
Predriver Supply Voltage	VDD	15	V
Power Dissipation	PD	2.5 <sup>note</sup>	W
Operating Temperature	TOPR	-40 ~ +85	°C
Storage Temperature	TSTG	-55 ~ +150	°C

### Note:

- When mounted on a 76.2mm × 114mm × 1.57mm PCB (Phenolic resin material).
- Power dissipation reduces 16.6mW/°C for using above Ta = 25°C
- Do not exceed PD and SOA (Safe operating area)

## Power Dissipation Curve



Ambient temperature, Ta[°C]

## Recommended Operating Condition (Ta = 25°C)

Parameter	Symbol	Value	Unit
Operating Supply Voltage	PVCC1, 2	4.5 ~ 13.2	V
Predriver Supply Voltage	VDD	4.5 ~ 13.2	V

## Electrical Characteristics (Ta = 25°C)

(Ta=25°C, VDD=PVCC1=PVCC2=8V, RL=8Ω, f=1kHz, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Quiescent Circuit Current1	IQ	Under no-load	-	17.0	25.0	mA
Internal Reference Input Voltage	VREF		3.40	3.70	4.0	V
Quiescent Circuit Current2 <sup>(Note1)</sup>	IPS	At Power Save On	-	10	100	μA
Power Save Off Voltage	VPSOFF		2.0	-	-	V
Power Save On Voltage	VPSON		-	-	0.5	V
<b>BTL DRIVER PART (CH1, CH2 and CH3)</b>						
Input High Level Voltage	VIH		2.4	-	VCC	V
Input Low Level Voltage	VIL		-0.3	-	0.5	V
Input High Level Current	IiH	V <sub>F</sub> =V <sub>R</sub> =5V	170	310	450	μA
Input Low Level Current (Forward)	IiLF	V <sub>F</sub> =0V	-10	-	0	μA
Input Low Level Current (Reverse)	IiLR	V <sub>R</sub> =0V	-50	-	0	μA
Output Offset Voltage	VOO		-30	-	30	mV
Maximum Output Voltage	VOM	V <sub>F</sub> =5V, V <sub>R</sub> =0V	4.4	5.0	5.6	V
Ripple Rejection Ratio <sup>(Note2)</sup>	RR	VRR=100mVrms, 100Hz	-	70	-	dB
<b>SPINDLE MOTOR DRIVER (CH4)</b>						
Input Bias Current	I <sub>B</sub>		-	10	300	nA
Output Offset Voltage	VOO4	CH4IN=OUTVREF	-50	-	50	mV
Maximum Output Voltage	VOM	CH4IN=4V	4.8	5.4	-	V
Closed-loop Voltage Gain	GVC		9.3	11.3	13.3	dB
Ripple Rejection Ratio <sup>(Note2)</sup>	RR	VRR=100mVrms, 100Hz	-	70	-	dB
<b>ANALOG SWITCH INPUT</b>						
Input High Level Voltage	VIHSW		2.0	-	VCC	V
Input Low Level Voltage	VILSW		-0.3	-	0.5	V
Input High Level Current	IiHSW	V <sub>SW</sub> =3.5V	-	60	90	μA
Input Low Level Current	IiLSW	V <sub>SW</sub> =0V	-10	0	10	μA
<b>OP-AMPLIFIER</b>						
Offset Voltage	VOFOP		-5	-	+5	mV
Input Bias Current	I <sub>BOP</sub>		-	10	300	nA
Output High Level Volatage	VOHOP		7.0	-	-	V
Output Low Level Volatage	VOLOP		-	-	0.2	V
Output Sink Current	I <sub>SINK</sub>		7.0	13.0	-	mA
Output Source Current	I <sub>SOURCE</sub>		2.0	9.0	-	mA
Open-loop Voltage Gain <sup>(Note2)</sup>	GVO	V <sub>IN</sub> =60dBV, 1KHz	-	65	-	dB
Slew Rate <sup>(Note2)</sup>	SR	f=50KHz, 2VPP(Squre)	-	0.5	-	V/us

### Note :

1. when the PS(pin20) is low level (under 0.5V) the bias circuit is disabled, so that the whole circuits are disabled.
2. Guranteed Design Value



# Application Information

## 1. Power Save Function

- Power save function is also performed at PS (pin20). The truth table is as follows:

SW (pin3)		PS (pin20)	
Input	Function	Input	Function
L	CAPA(pin25) OFF	L	Power Save ON
H	CAPA(pin25) ON	H	Power Save OFF

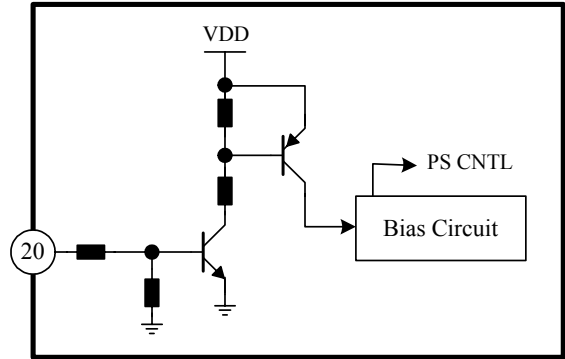


Figure 1. Truth table of Gain selection and Mute Function

- When the PS (pin 20) is high level (above 2V), the bias circuit is enable. On the other hand, when the PS(pin20) is low level (under 0.5V), the bias circuit is disabled.
- When the CAPA(pin3) is low level, the CAPA (pin25) is opened in Figure. 4.

## 2. TSD (Thermal Shutdown) Function

- When the chip temperature rises above 175°C, then the 4-channels BTL driver output circuit will be muted. The TSD circuit has the hysteresis temperature of 25°C.

## 4. Balanced Transformerless(BTL) Driver (CH1, CH2 and CH3)

- CH1, CH2 and CH3 drive parts are composed of internal filter, V-I converter and output power amplifiers.

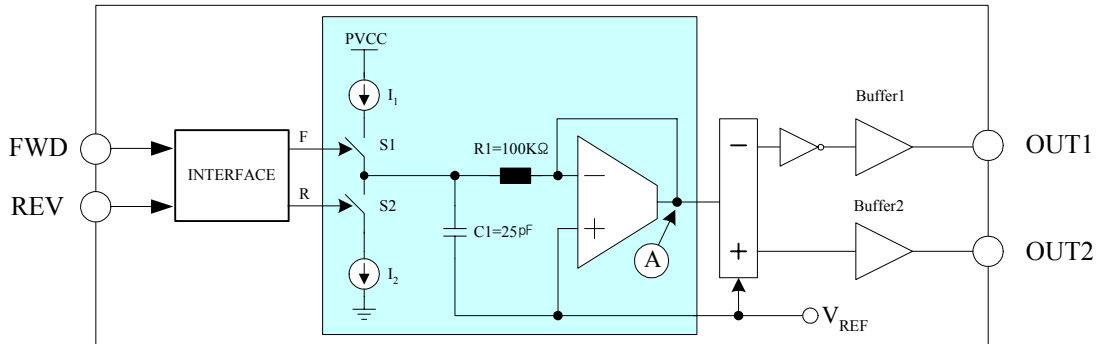


Figure 2. Schematic of BTL Driver (CH1, CH2 and CH3)

F	R	S1	S2
L	L	OFF	OFF
L	H	OFF	ON
H	L	ON	OFF
H	H	ON	ON

H : above 2.4 [V]  
L : under 0.5 [V]

Table 1. Truth table of internal switches operation

- Internal primary filter is composed of sourcing/sinking current source of 25uA and forward/reverse controlled switches.
- It converts "FWD/REV" digital signals to analog signal as shown Figure. 2.

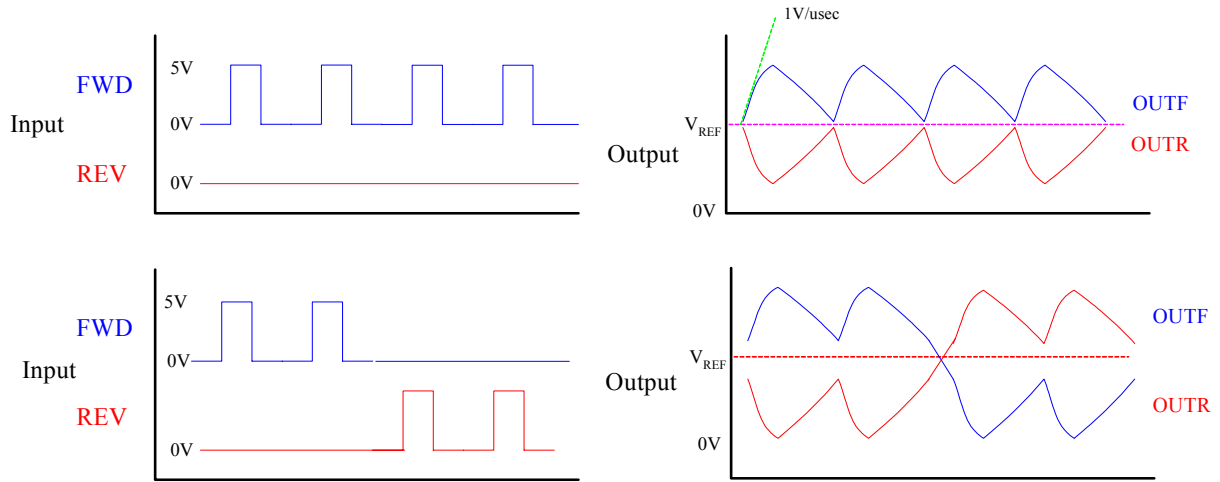


Figure 3. Operation waveforms of BTL Driver (CH1, CH2 and CH3)

- If the forward input signal is high level (above 2.4V) and reverse input signal is low level (under 0.5V), then the forward current source switch S1 and reverse current source switch S2 become turn-on and turn-off, respectively.
- This causes the internal capacitor, C1, to be charged with sourcing current source of 25uA and consequently the voltage of the filter output,  $V_A$ , increases with the internal time constant of 2.5usec.
- 

$$V_A = I_1 \times R_1 \approx 2.5[V], \quad (\text{Or reverse input} : -2.5[V])$$

- The time constant is

$$R \times C = 2.5[\mu \text{sec}]$$

Where, R is 100 [kΩ] and C is 25[pF].

- The output voltages of power amplifiers,  $V_{OUTF}$  and  $V_{OUTR}$ , are given as:
- 

$$V_{OUTF} = V_{REF} + V_A \quad [V]$$

$$V_{OUTR} = V_{REF} - V_A \quad [V]$$

## 5. Channel 4 Driver (Spindle Motor Driver)

- The channel 4 driver is composed of input amplifier with input selection switch, V-I converter and output power amplifiers.
- The voltage,  $V_{REF}$ , is the external reference voltage given by the bias voltage of the pin 26 in Figure. 4.
- The input signal,  $V_{IN}$ , through the CH4IN (pin24) is amplified by 100K/100K times and then fed to the next amplifier. And the amplified voltage is amplified by  $R2/R1$  times and then the fed to the level shift circuit.
- Level shift produces the current due to the difference between the input signal and the internal power reference ( $PVCC/2$ ). The current produced as  $+\Delta I$  and  $-\Delta I$  is fed into the driver buffer.
- If it is desired to change the gain, then the CH4CAPA (pin25) can be used. It is controlled by the SW (pin3) input signal.
- When the SW (pin3) is high level, then the input voltage,  $V_{IN}$ , applied to the CH4CAPA (pin25).

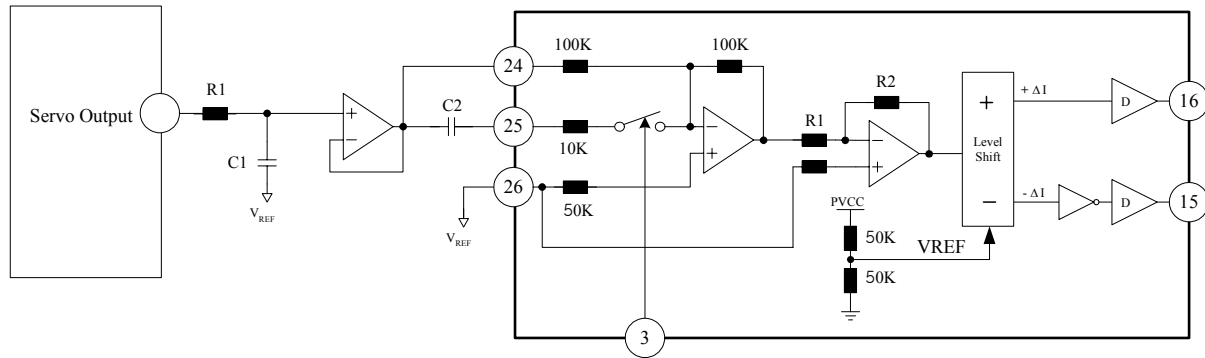
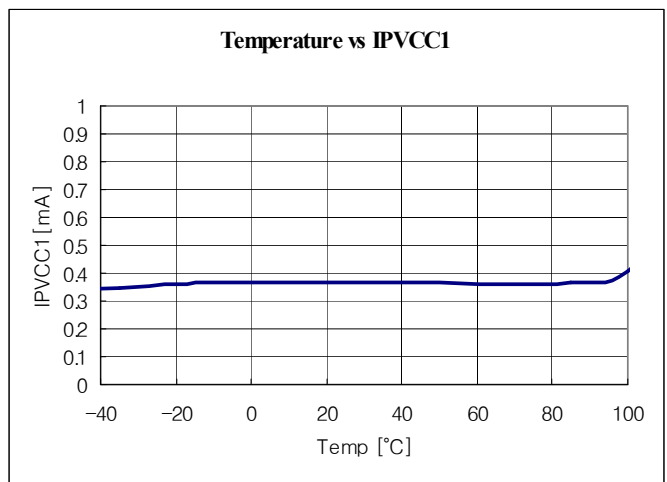
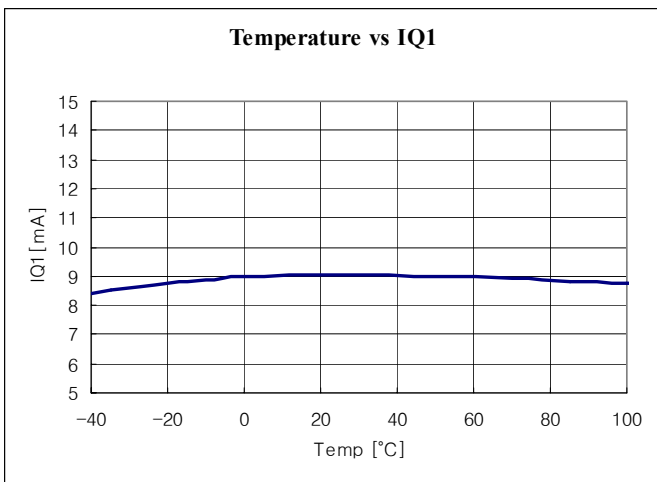
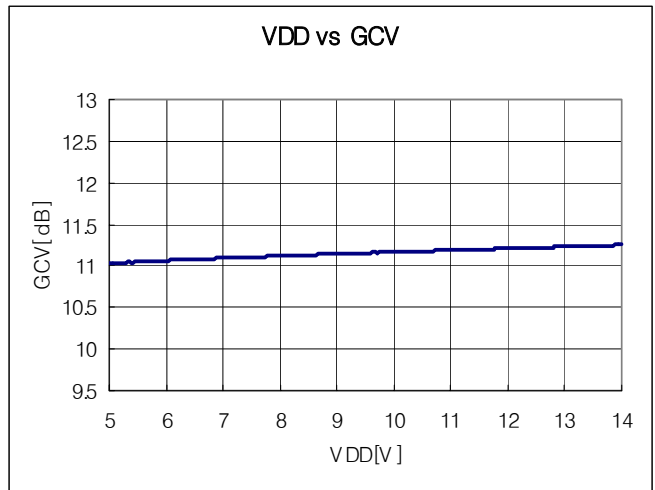
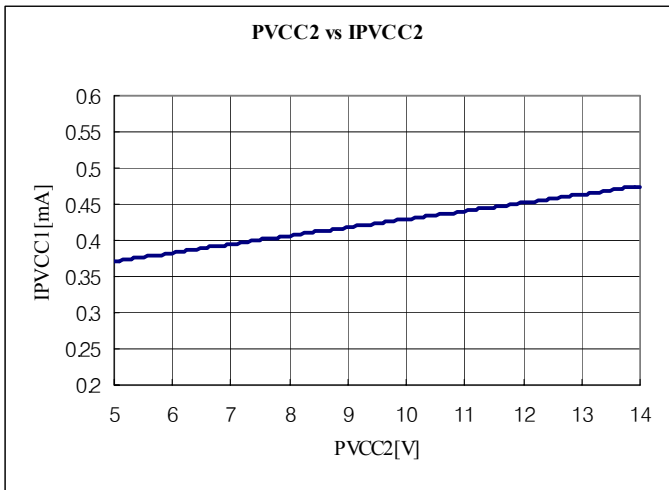
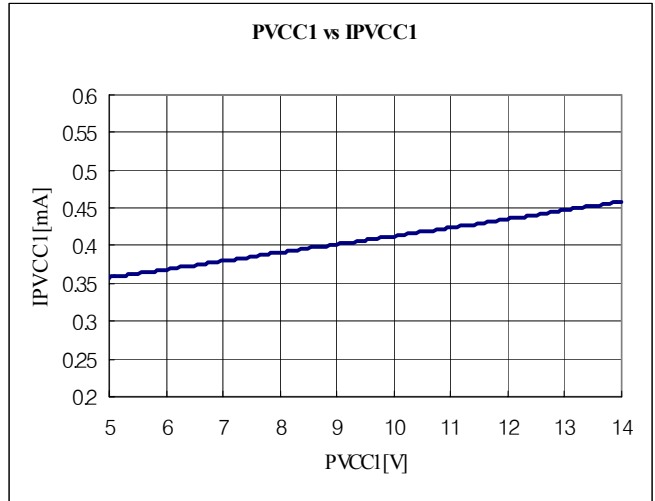
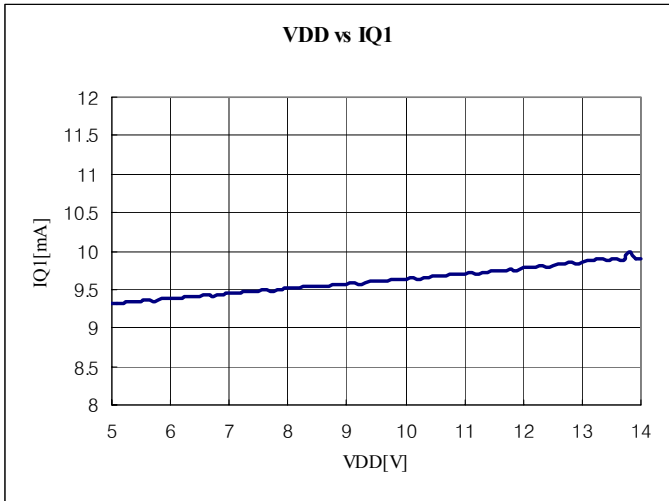
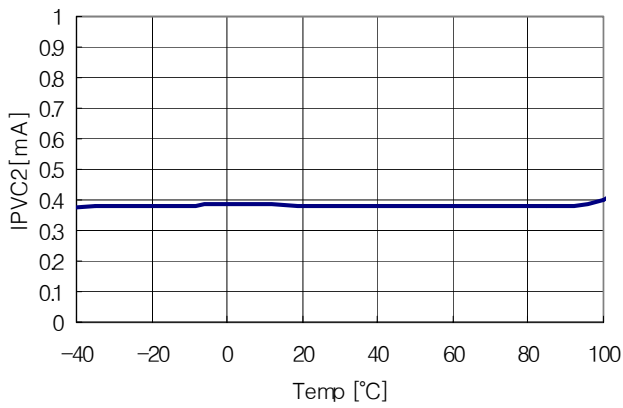


Figure 4. Channel 4 Spindle Driver

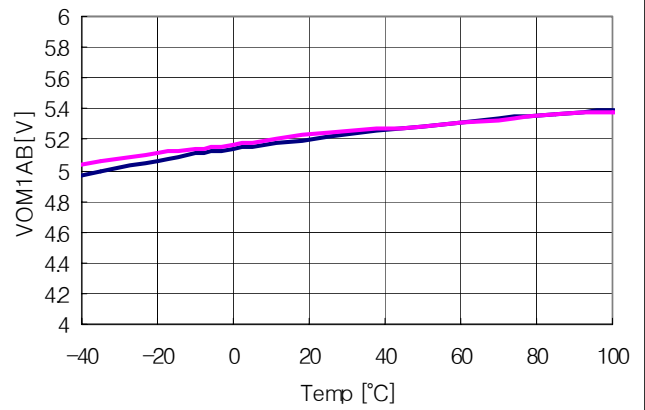
## Typical Performance Characteristics



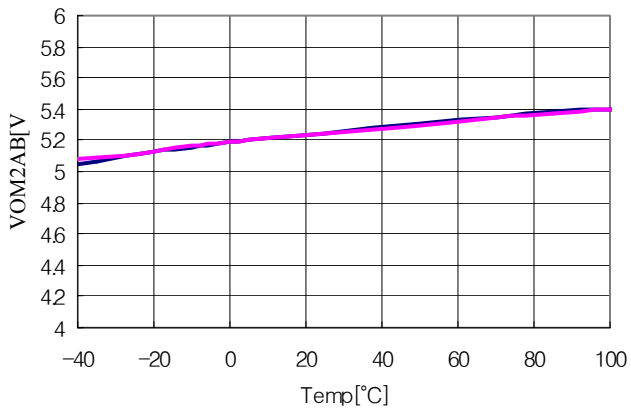
Temperatur vs IPVCC2



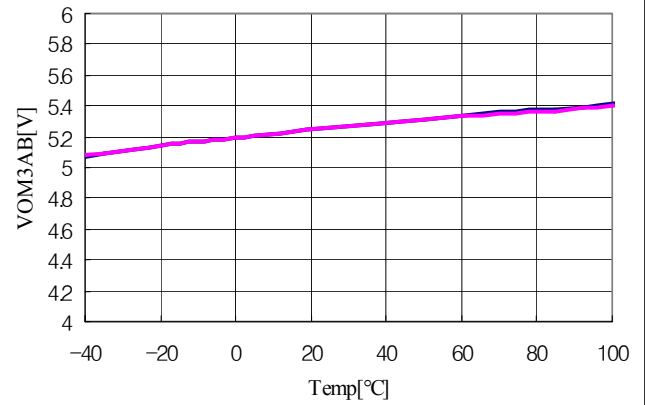
Temperature vs VOM1AB



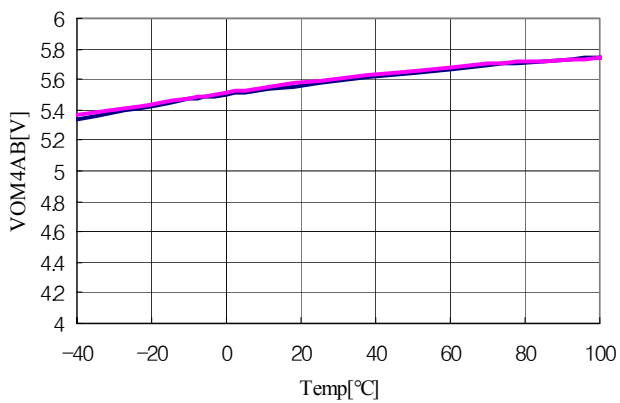
Temperature vs VOM2AB



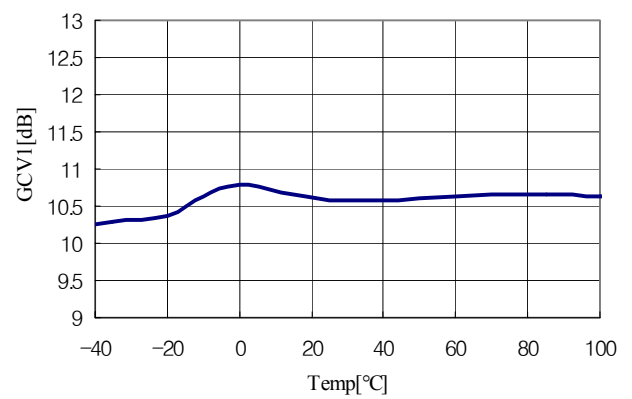
Temperature vs VOM3AB

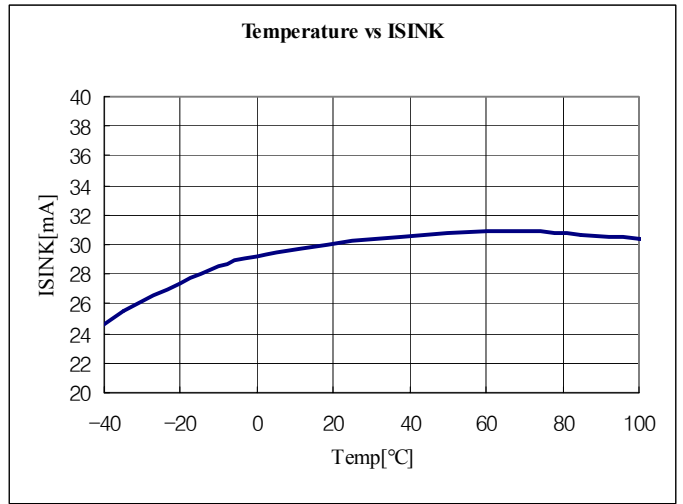
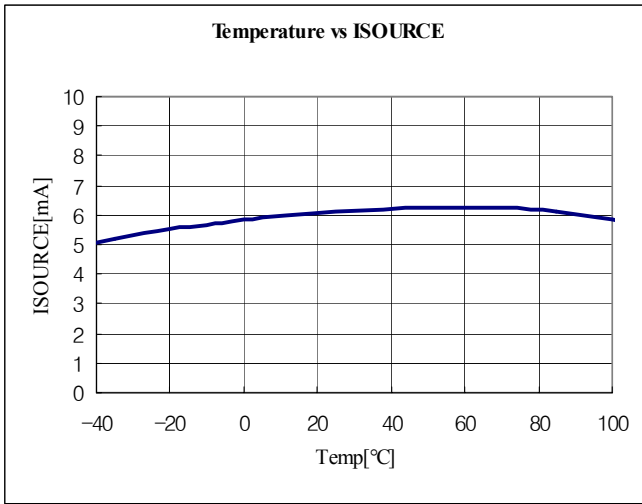


Temperature vs VOM4AB

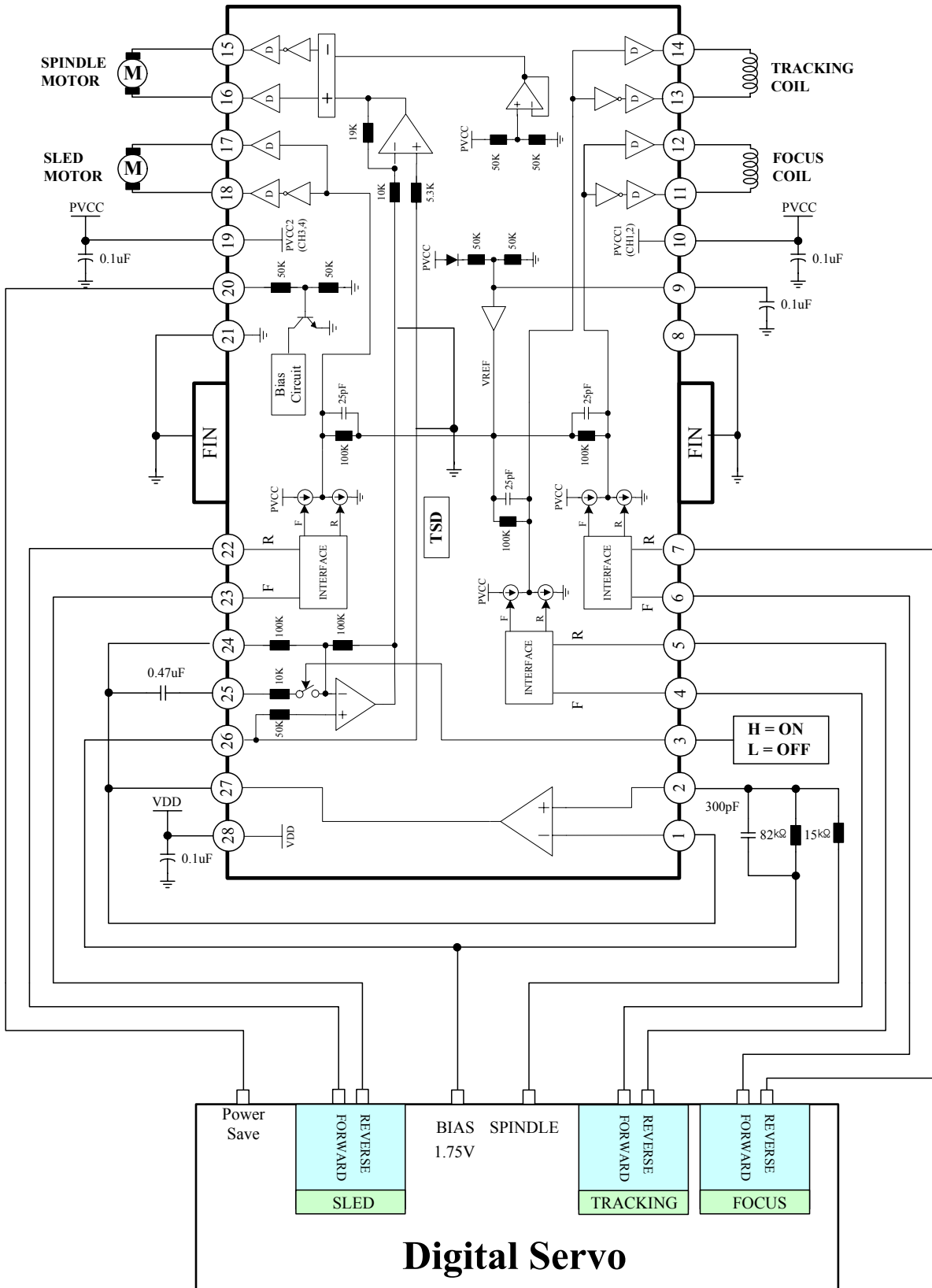


Temperature vs GCV1





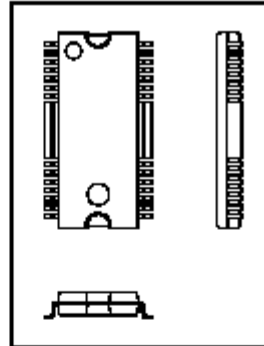
# Typical Application Circuits



# Mechanical Dimensions(Unit : mm)

## Package Dimensions

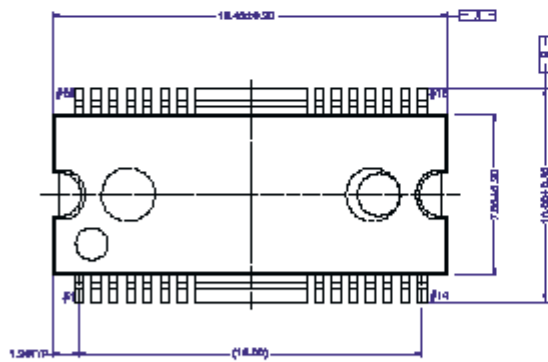
### 28-SSOPH-375SG2



Scale 1:1 on letter size paper

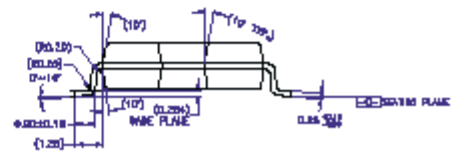
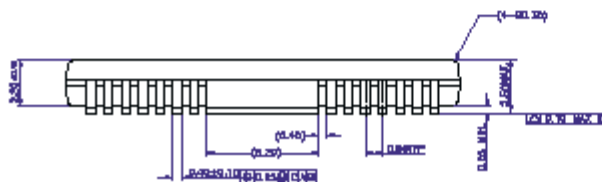
Dimensions shown below are in:  
inches [millimeters]

Part Weight per unit (gram): 0.65



NOTE :

1. CONTROLLING DIMENSIONS ARE MM ( ) IS REFERENCE
2. DIMENSIONING AND TOLERANCING PER ANSI Y 14.8M - 1982.
3. "A" AND "B" ARE REFERENCE DIMENSIONS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH/PROTRUSIONS. MOLD FLASH/PROTRUSIONS AT "A" SHALL NOT EXCEED 0.152MM(0.006") PER SIDE. INTER-LEAD FLASH/PROTRUSIONS AT "B" SHALL NOT EXCEED 0.254MM(0.010") PER SIDE.
4. PIN NUMBERS START WITH PH #1 AND CONTINUE COUNTERCLOCKWISE TO PH #28 WHEN VIEWED FROM TOP.





**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.